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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/685,362	10/10/2000	Holger Hubner	GR 98 P 1513	3999

7590 06/02/2003

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EXAMINER
WARREN, MATTHEW E

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 06/02/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/685,362	HUBNER ET AL.	
	Examiner	Art Unit	
	Matthew E. Warren	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

P riod for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 March 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4 and 6-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4, 6-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

This Office Action is in response to the Amendment filed on March 17, 2003.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4, and 6-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ryan et al. (US 5,972,788) in view of Leung et al. (US 5,563,762).

Ryan et al. shows (figs. 1-3) semiconductor component comprising a first metal layer (M1) forming a first metal area (21) and a second metal area (24) electrically isolated from each other. A dielectric layer (16) is formed over the first metal area. A second metal layer (M2) forms a third metal area (22) insulated from the first metal layer by an interposition of said dielectric layer (16), the second metal layer together with the dielectric layer and the first metal area form a memory element (capacitor). The second metal layer (M2) further forms a fourth metal area (25) which together with the second metal area (24) forms a contact area to make contact with the second metal layer (metal 34 connects metal layers 25 and 24 together). An additional insulating layer (31) is formed over a contact (25 and 24). An opening is formed in the insulating layer and is filled with conductive material (34) to form an external connection to the contact area. The fourth metal area (25) is separated from the second metal area (24) by interposition

of the dielectric layer (16). One further opening (33) is formed in the insulation layer. With respect to the limitations of claim 2, the contact area of combined cited references inherently forms an etching resist because it has the same structure and materials as the instant invention. Ryan et al. shows all of the elements of the claims except the fourth metal area making direct contact with the second metal area, the second metal layer having a connection between the third and fourth metal area, and the various materials used to form the metal and dielectric layers. Leung et al. shows (fig. 3) a semiconductor component having a capacitor structure (128, 130, and 134) and a contact area having a fourth metal area (134) in direct contact with a second metal area (126). The capacitor has an electrically conductive connection between the third metal area (134) of the capacitor and the fourth metal area of the contact structure (134) because each area is formed simultaneously by the second layer (134). With this configuration, interconnection is made simultaneously with the capacitor top electrode and the contact area to underlying metallization without disrupting routing of the underlying interconnect (col. 8, lines 30-48). The first and second metal layers are composed of a noble metal including platinum and the dielectric is composed of a ferroelectric (col. 11, line 43-col. 12, line 4). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the capacitor and contact structure of Ryan by forming the connection between the capacitor top electrode and contact portion simultaneously as taught by Leung to simplify the interconnection process and form a capacitor structure above the semiconductor without disrupting routing of the underlying interconnect metallization.

With respect to the etching process of claim 2, a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, **190 USPQ 15 at 17**(footnote 3). See also in re Brown, **173 USPQ 685**: In re Luck, **177 USPQ 523**; In re Fessmann, **180 USPQ 324**: In re Avery, **186 USPQ 116** in re Wertheim, **191 USPQ 90** (**209 USPQ 254** does not deal with this issue); and In re Marosi et al, **218 USPQ 289** final product per se which must be determined in a "product by, all of" claim, and not the patentability of the process, and that an old or obvious product, whether claimed in "product by process" claims or not. Note that Applicant has the burden of proof in such cases, as the above case law makes clear. "Even though product-by- process claims are limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process." In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985)(citations omitted).

Response to Arguments

Applicant's arguments filed with respect to claims 1-9 have been fully considered but they are not persuasive. The applicant primarily argues that the capacitor of Ryan et al. is not a memory element but a capacitor for analog devices and that Leung et al. cannot be combined with Ryan because Leung provides an on-chip capacitor. The examiner believes that the cited references show all of the elements of the claims and

that they can be combined because they are analogous art. With respect to the argument that the capacitor of Ryan is not a memory element, Ryan discloses in column 7, lines 49-63 that the capacitor and interconnect is employed in integrated circuits. It is well known in the art that memory elements in semiconductor integrated circuits use capacitors. Furthermore, the claims of the applicant's invention broadly recite that the "third metal area together with said dielectric and first metal area forms a memory element." Thus the layers of Ryan's capacitor also forms a memory element because they are formed of the same materials and have the same structure as the applicant's claimed invention.

Although the capacitor of Leung is an on-chip capacitor and Ryan discloses an integrated circuit memory capacitor, it can still be combined with Ryan because both are capacitors. The Leung reference deals with forming capacitors and interconnects simultaneously. As seen from the figures, the second metal layer (134) is connected as the capacitor top electrode and as part of the interconnect (over 126). With such a configuration, the activation of the capacitor simultaneously provides a voltage to the interconnect or a voltage to the interconnect simultaneously activates the capacitor. One of ordinary skill in the art would apply this teaching to Ryan to reduce the number of connections and vias to the interconnect and the capacitor of Ryan thus reducing process steps and manufacturing costs. In column 9, lines 30-48 of Leung, it is also taught that the on-chip capacitor and interconnect is formed without disrupting routing of underlying interconnects. It can also be inferred that the interconnect and capacitor allow for a larger packing density because there are less vias and interconnect portions.

The on-chip capacitor and interconnect of Leung are applicable to integrated circuit of Ryan and Leung shows motivation for combining. The cited references show all of the elements of the claims and this action is made final.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew E. Warren whose telephone number is (703) 305-0760. The examiner can normally be reached on Mon-Thurs, and alternating Fri, 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703) 308-1690. The fax phone numbers for

the organization where this application or proceeding is assigned are (703) 305-3432 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

MEW
May 28, 2003

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800